2/4 B.Tech FIRST SEMESTER

IT3T2 **COMPUTER ORGANIZATION** **Credits: 4**
(Common to CSE/IT)

Lecture: 4 Periods/week **Internal assessment: 30 marks**
Tutorial: 1 Period /week **Semester end examination: 70 marks**

Objectives:

- To have a thorough understanding of the basic structure and operation of a digital computer.
- To design the control unit in detail including hardware for the micro programmed sequencer.
- To have a thorough understanding of the central processing unit and various instructions formats together with a variety of addressing modes.
- To discuss in detail the operation of the arithmetic unit including the algorithms & implementation of fixed-point and floating-point addition, subtraction, multiplication & division.
- To explain the hierarchical memory system including cache memories and virtual memory
- To discuss the different ways of communicating with I/O devices and standard I/O interfaces.
- To demonstrate the concept of pipelining and the way it can speed up the processing, Instruction pipelining and RISC pipelining.
- To study the basic characteristics of Multiprocessors and Interconnection structures and Interprocessor communication.

Outcomes:

Students will be able to:

- Understand the basic structure of a digital computer
- Design the control unit in detail including hardware for the micro programmed Sequencer.
- Learn the various instructions format together with a variety of addressing modes.
- Perform Arithmetic operations of binary number system.
- Know the organization of the Control unit, Arithmetic and Logical unit, Memory unit and the I/O Unit.
- Understand the concept of Pipelining and the way it can speed up the processing.
- Understand the basic characteristics of Multiprocessors and Interconnection structures and the need of Interprocessor communication.

Syllabus:

UNIT-I

REGISTER TRANSFER AND MICRO-OPERATIONS:

Register Transfer Language, Register Transfer, Bus and memory Transfers, Arithmetic Micro-operations, Logic Micro-operations, Shift Micro-operations, Arithmetic Logic Shift Unit.

UNIT-II

BASIC COMPUTER ORGANIZATION AND DESIGN:

Instruction codes, Computer Registers, Computer Instructions, Timing and Control, Instruction cycle, Memory-Reference Instructions, Input-Output and Interrupt, Design of Basic Computer.

UNIT-III

MICRO PROGRAMMED CONTROL:

Control Memory, Address Sequencing, Micro-Program example, Design of Control Unit.

CENTRAL PROCESSING UNIT:

General register Organization, Stack Organization, Instruction Formats, Addressing Modes, Data Transfer and Manipulation, Program Control, Reduced Instruction Set Computer (RISC).

UNIT-IV

COMPUTER ARITHMETIC:

Addition and Subtraction, Multiplication Algorithms, Division Algorithms, Floating-point Arithmetic operations.

UNIT-V

MEMORY ORGANIZATION:

Memory Hierarchy, Main Memory, Auxiliary memory, Associative Memory, Cache Memory, Virtual Memory, Memory Management hardware.

UNIT-VI

INPUT-OUTPUT ORGANIZATION:

Peripheral Devices, Input-output Interface, Asynchronous Data Transfer, Modes of Transfer, Priority Interrupt, Direct Memory Access (DMA),Input-Output Processor, Serial Communication.

UNIT-VII

PIPELINE AND VECTOR PROCESSING:

Parallel processing, Pipelining, Arithmetic pipeline, Instruction pipeline, Risc pipeline.

UNIT-VIII

MULTIPROCESSORS:

Characteristics of multiprocessors, Interconnection structures, Inter processor arbitration, Interprocessor communication and synchronization.

Text books:

1. 'Computer System Architecture', Morris M. Mano, 3rd edition,Prentice Hall India.

Reference books:

1. Computer Organization and Achitecture, William Stallings ,8th edition,PHI
2. Computer Organization, Carl Hamachar, Vranesic, McGraw Hill.